Evolvable Hardware Solutions for Extreme Temperature Electronics

A. Stoica, D. Keymeulen, and R. Zebulum
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, CA 91109
adrian.stoica@jpl.nasa.gov

Abstract

Temperature and radiation tolerant electronics, as well as long life survivability are key capabilities required for future NASA missions. Current approaches to electronics for extreme environments focus on component level robustness and hardening. Compensation techniques such as bias cancellation circuitry have also been employed. However, current technology can only ensure very limited lifetime in extreme environments. This paper presents a novel approach, based on evolvable hardware technology, which allows adaptive in-situ circuit redesign/reconfiguration during operation in extreme environments. This technology would complement material/device advancements and increase the mission capability to survive harsh environments. The approach is demonstrated on a prototype chip, which recovers functionality at 250°C. Besides the applications that provide adaptive reconfiguration, evolutionary algorithms can be used to automatically design (fixed) circuits for high temperatures. While simulations show that conventional AND gate design fails at high temperatures such as 320°C, evolution is able to synthesize AND gate circuits operating accurately at this temperature.

1. Introduction

In-situ planetary exploration requires extreme-temperature electronics able to operate in low temperatures, such as below –220°C on Neptune (-235°C for Triton and Pluto) or high temperatures, such as above 470°C as needed for operation on the surface of Venus. Extrapolations of current developments indicate that hot electronics technology for >400°C environments may not be ready in time for the 2006-2007 missions, except possibly for "grab-and-go" or "limited life" operations [1]. For extended missions, innovative approaches are needed. Terrestrial applications include combustion systems, well logging, nuclear reactors and dense electronic packages.

The maximum working temperature for semiconductors can be estimated from their intrinsic carrier density, which depends on the band-gap of the material. When the intrinsic density reaches the doping level of the devices, electrical parameters are expected to change drastically [2]. For high-voltage regime (1000V) the theoretical limit for silicon is 150°C; for discrete devices below 100V it is expected about 250°C [2]. Materials used up to 300°C include bulk silicon and silicon on insulator (SOI) technologies; for higher temperatures gallium arsenide (GaAs), silicon carbide (SiC) and diamond show promise, and devices have been demonstrated at 500°C [3] A survey of high-temperature effects and design considerations is found in [4]. A review of the physical limits and lifetime limitations of semiconductor devices at high-temperatures is found in [2].

In addition to material/device solutions, circuit solutions for the compensation of the effects of temperature have also been employed. Circuit solutions that compensate offset voltage and current leakage problems are described for example in [3], where several circuit topologies for high-temperature design, including a continuous-time auto-zeroed OpAmp and an A/D circuit that uses error suppression to overcome high-temperature leakages, are given. Another circuit for high-temperature operation with current leakage compensation is presented in [5]. Bias cancellation techniques for high-temperature analog application are presented in [6].

All the above solutions are fixed circuit design solutions, and satisfy the operational requirements only over a given temperature range. Once the limits of the range are exceeded the performance deteriorates and cannot be recovered. In this paper we propose the use of reconfigurable chips, which allow for a large number of topologies to be programmed, some more suitable for high-temperature. The interconnections between components can be changed, and new circuits can be configured, in an arrangement that uses the on-chip components/devices *at the new operational point on their characteristics.* In essence, a new design process takes place automatically, in-situ, under the control of a search algorithm. The configurations for different operational points could be determined either before launch - part of the original design (which would identify good configurations and store them in a memory) - or in-situ. At the higher temperatures, once the performance of the current topology starts to deteriorate, the system would switch to a more suitable topology.

Reconfiguration can be controlled by evolutionary algorithms. Thompson *et al*. used Genetic Algorithms in a first on-chip evolution on a reconfigurable device (a Field Programmable Gate Array (FPGA)) [7], in which they evolved a frequency discriminator. Their early experiments involved also a temperature aspect, although in a different perspective than the focus of this paper. The circuits that emerged as solutions to the frequency discrimination experiments were very sensitive to the temperature, basically functioning only at the temperature for which they were evolved. To overcome this problem, and obtain circuits with some degree of robustness they evaluated each chromosome downloaded into FPGAs placed at different temperatures (they tested at -27^{o}C, $+27^{o}$C, $+60^{o}$C). The fitness assigned to the chromosome corresponded to the worst behavior in the tested conditions. At the end, the evolved circuits operated over the entire range of temperatures.

While Thompson's focus was finding a single topology with satisfactory stability with temperature (in a range over which perhaps one can find a unique robust solution for the whole domain), the focus of our research is to obtain circuits exceeding known limits of extreme temperature electronics, in which the device characteristics have changed dramatically compared to normal temperatures. It's unlikely that a unique circuit design solution will exist covering both normal and extreme temperatures, since devices/components behave very differently at extreme temperatures. Our focus is on adaptation by reconfiguration to the topology that is suitable for the extreme temperature.

As part of an effort to develop evolution-oriented devices for EHW experiments, we designed and fabricated a series of Field Programmable Transistor Array (FPTA) chips in 0.5 micron and 0.18 micron bulk CMOS. These chips are reconfigurable at transistor level and were used to demonstrate on-chip evolution/synthesis of a variety of conventional building blocks for electronic circuits such as logical gates, transconductance amplifiers, filters, Gaussian neurons, data converters, etc [8], [9].

The chips were also tested at low and high temperatures and with injected faults [10] to observe how functionality degrades and how it can be recovered through evolutionary self-configuration. As part of a paper [11] addressing several evolutionary experiments, we presented preliminary results on using evolution to recover the functionality of FPTA-mapped circuits affected by changes in temperature. In that note, the DC transfer function of a Gaussian circuit was recovered by evolutionary synthesis, after being deteriorated by the low (-196^{o}C) temperature in one experiment and high ($+250^{o}$C) temperature in another. The temperature has caused deviations of the analog curve response. In this paper we present a more detailed account of the evolutionary recovery, and explain how temperature degradation can fundamentally impact the intended function of the IC. The example chosen illustrates a digital circuit, with an output that toggles at the temperature increase, thus totally altering the intended logical function. Evolution is able to find alternate circuits that perform correctly at the higher temperature.

The paper is organized as follows: Section 2 presents the details on a FPTA chip developed as an evolution-oriented architecture for reconfigurable hardware, and introduces the experimental testbed. Section 3 presents experiments that illustrate that evolution-guided reconfiguration can recover functionality deteriorated/altered by increased temperature. Section 4 illustrates the evolution of circuits specifically designed for high temperatures. Section 5 presents discussion and conclusions.

2. The FPTA and Experimental Setup

The idea of an FPTA was introduced first in [8]. The FPTA is a concept design for hardware reconfigurable at transistor level. As both analog and digital CMOS circuits ultimately rely on functions implemented with transistors, the FPTA is a versatile platform for the synthesis of both analog and digital (and mixed-signal) circuits. Further, it is considered a more suitable platform for synthesis of analog circuitry than existing FPGAs or Field Programmable Analog Arrays (FPAAs), extending the work on evolving simulated circuits to evolving analog circuits directly on the chip. The FPTA cell is an array of transistors interconnected by programmable switches. The status of the switches (ON or OFF) determines a circuit topology and consequently a specific response. Thus the topology can be considered as a function of switch states, and can be represented by a binary sequence, such as "1011…", where by convention one can assign 1 to a switch turned ON and 0 to a switch turned OFF. Figure 1 illustrates an example of a FPTA module consisting of 8 transistors and 24 programmable switches. In this example, transistors P1-P4 are PMOS, and N5-N8 are NMOS. Programming the switches ON and OFF defines a circuit for which the effects of non-zero, finite impedance of the switches can be neglected in the first approximation. The experiments in this paper were performed on our first chips, which were fabricated in 0.5 micron CMOS.

The experimental testbed consists of testing boards connected by data acquisition boards to a PC and to a supercomputer. The system is described in detail in [12]. For the purpose of the temperature experiments we have constructed special boards, which were inserted in temperature chamber for high temperature and in liquid nitrogen for low temperatures.

3. Recovery by Reconfiguration

Experiments were carried both in simulations and with the chip immersed in temperature controlled environments at low temperatures (as low as -196^{o}C) and high temperature (up to $+250^{o}$C). The sequence of steps was: (1)

Implement a human design or evolve a new design for desired function at 27°C. (2) Expose chip to low or high temperature and observe degraded response (3)Apply evolution to obtain a new circuit solution that recovers functionality. In these experiments the following evolutionary parameters were used: Population size of 50, running for 200 generations; mutation rate of 8% and crossover rate of 30%.

We have recorded response degradation, both at –196°C and 250°C, for a variety of analog and digital circuits including multipliers, gaussian-shape curve generators, and logic gates. In all cases evolution recovered functionality, by finding a new circuit solution (interconnection pattern).

Figure 2 illustrates an evolved AND gate at 27°C and its degrading response at 160, 170 and 180°C. Figure 3 illustrates a solution that recovers functionality. These are results from Spice simulations. Figure 4 and 5 illustrate experiments with the real chips. Figure 4 presents an oscilloscope capture that illustrates the degradation with temperature in response of an AND gate. One should remark that the evolved solutions, while adapted to the extreme temperature, were not necessarily preserving functionality when the temperature was being brought back to room temperature. Figure 5.a. shows the recovered functional response, while 5.b and 5.c. show how that circuit itself losses adaptation once temperature gets back to the original one (for which the original circuit becomes more suitable).

4. Custom hot electronics designs

Standard AND gates were preserving functionality at 250°C. Simulations with default SPICE models indicate that degradation occurs around 300°C (this is for DC levels or low frequency tests, high frequency response will likely degrade before that). Standard gate and its degraded behavior at 320°C are illustrated in Figure 6. We used evolution to obtain a design that would accurately operate at 320°C. (Figure 7).

5. Discussion and Conclusions

The experiments, albeit simple, demonstrate the possibility of using evolutionary self-configuration to recover functionality lost at extreme temperatures. In addition evolutionary design can be used to create designs targeted to the extreme temperatures. One should mention here that while a device may work at a certain temperature, the real limiting factors for applications will be failure rates and lifetimes. The experiments were performed on bulk CMOS because of the convenience and low cost of fabricating in this technology. For maximum performance evolvable hardware should make use or be an enhancing technique combined with materials/devices more appropriate for extreme temperatures, such as SiC, etc.

Acknowledgements

The work described in this paper was performed at the Center for Integrated Space Microsystems, Jet Propulsion Laboratory, California Institute of Technology and was sponsored by the National Aeronautics and Space Administration and the Defense Advanced Research Projects Agency.

References

[1] – Proceedings of the NASA/JPL Conference on Electronics for Extreme Environments, Feb. 9-11, 1999; Pasadena, CA. In http://extremeelectronics.jpl.nasa.gov/conference".

[2] - Wondrak, W. Physical Limits and Lifetime, “Limitations of Semicondctor Devices at High Temperatures”, Microelectronics Reliability 39 (1999) 1113-1120.

[3] J. Haslett, F. Trofimenkoff, I. Finvers, F. Sabouri, and R. Smallwood, "High Temperature Electronics Using Silicon Technology", 1996 IEEE Solid State Circuits Conference, pp. 402-403.

[4] - Shoucair, F., “Design considerations in high temperature analog MOS integrated circuits”. IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 9(3):242, 1986.

[5] Mizuno, K., N. Ohta, F. Kitagawa , H., Nagase, E., “Analog CMOS Integrated Circuits for High-Temperature Operation with Leakage Current Compensation”, 4th International High Temperature Electronics Conf., Albuquerque, p. 41, 1998.

[6] F. Shi, "Analyzing Bias Cancellation Techniques for High temperature Analog Applications", 4th International High Temperature Electronics Conf., Albuquerque, pp. 172-175, 1998.

[7] Adrian Thompson and Paul Layzell, “Evolution of Robustness in an Electronics Design” ICES 2000, LNCS 1801, pp. 218-228, Edinburgh, UK, April, 2000.

[8] A. Stoica, “Toward evolvable hardware chips: experiments with a programmable transistor array”, Proceedings of 7th International Conference on Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, Granada, Spain, April 7-9, IEEE Comp Sci. Press, 1999, 156-162.

[9] A. Stoica, R. Zebulum, D. Keymeulen, R. Tawel, T. Daud, and A. Thakoor, “Reconfigurable VLSI Architectures for Evolvable Hardware: from Experimental Field Programmable Transistor Arrays to Evolution-Oriented Chips”, IEEE Transactions on VLSI Systems, February 2001,227-232.

[10] Keymeulen, D., Stoica, A., Zebulum, R., Jin, Y., “Fault-Tolerant Evolvable Hardware using Field Programmable Transistor Arrays”. In IEEE Transactions on Reliability, Special Issue on Fault-Tolerant VLSI Systems, vol. 49, No. 3, 2000 September, pp. 305-316,. IEEE Press.

[11] A. Stoica, D. Keymeulen, R. Zebulum, A. Thakoor, T. Daud, G. Klimeck, Y. Jin, R. Tawel and V. Duong, “Evolution of analog circuits on Field Programmable Transistor Arrays”, Proc. of the Second NASA/DOD Workshop on Evolvable Hardware, Palo Alto, CA, July 13-15, 2000, IEEE Computer Society Press, pp. 99-108

[12] D. Keymeulen, G. Klimeck, R. Zebulum, A. Stoica, and C. Lazaro., “EHWPack: A Parallel Software/Hardware Environment for Evolvable Hardware” In Whitley Darrell (eds.), Proceedings of of(GECCO-2000, July 8-12, 2000, Las Vegas, Nevada USA. San Francisco, CA: Morgan Kaufmann.

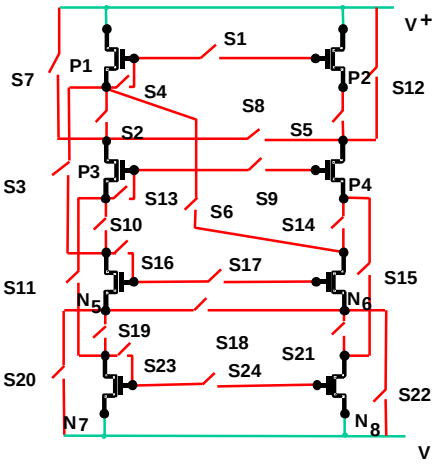


Figure 1 - Field Programmable Transistor Array Cell.

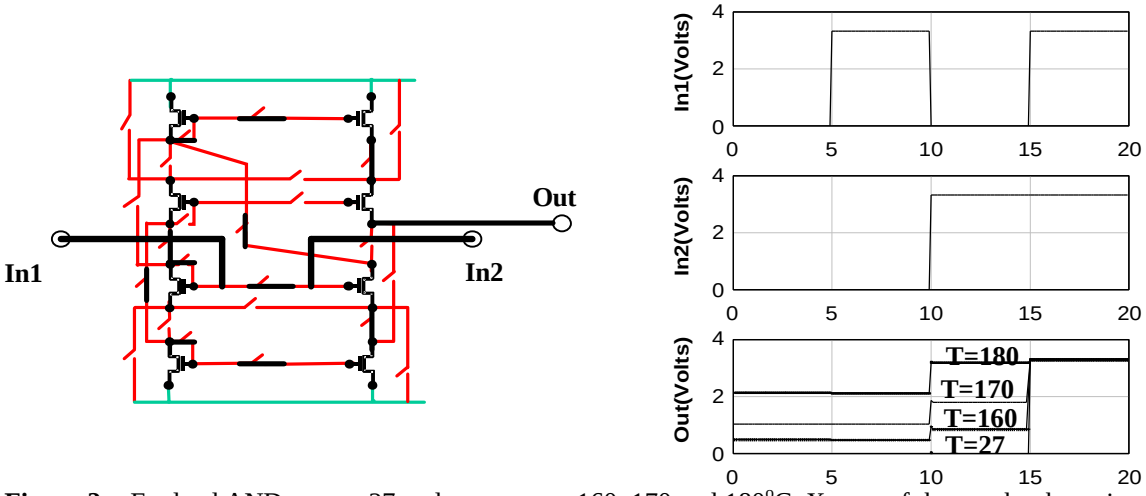


Figure 2 - Evolved AND gate at 27 and response at 160, 170 and 180°C**.** X axes of the graphs show time in ms.

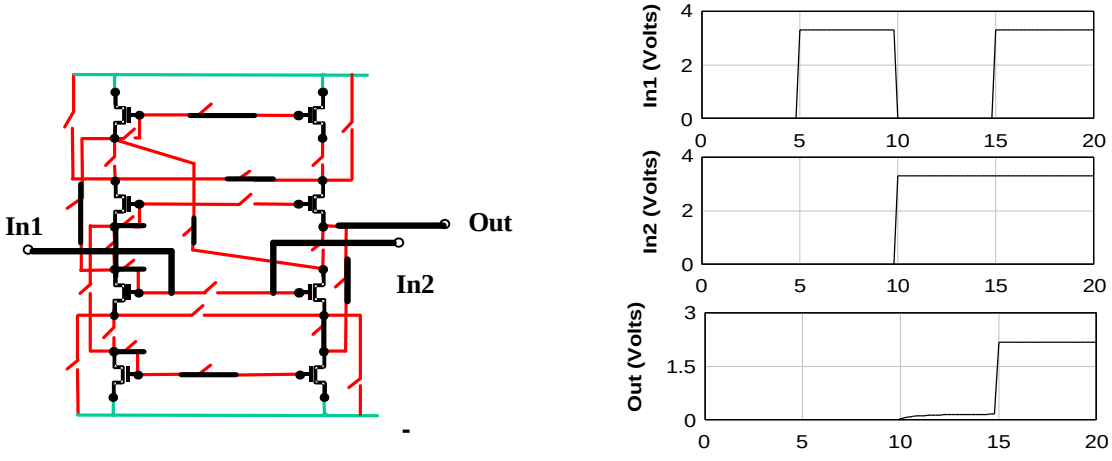
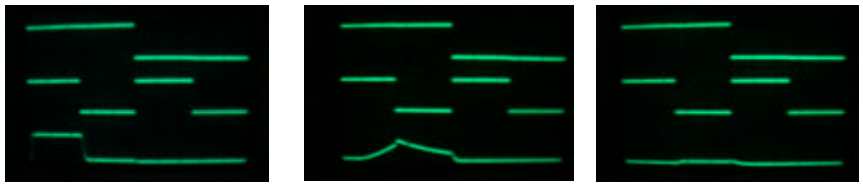


Figure 3 - Recovered AND gate at 180°C. X axes of the graphs show time in ms.

a) b) c)

Figure 4. Response of AND gate evolved at 27°C when measured at: a) 27°C, b) 100°C, c) at 250°C. The top and middle waveforms are the inputs, the bottom one is the output, which should be 'high' only when both inputs are 'high'.



a) b)

Figure 5 - Response of AND gate evolved at 250°C and measured at a) 250°C, b) 150°C, c) at 137° C. The top and middle waveforms are the inputs, the bottom one is the output, which should be 'high' only when both inputs are 'high'.

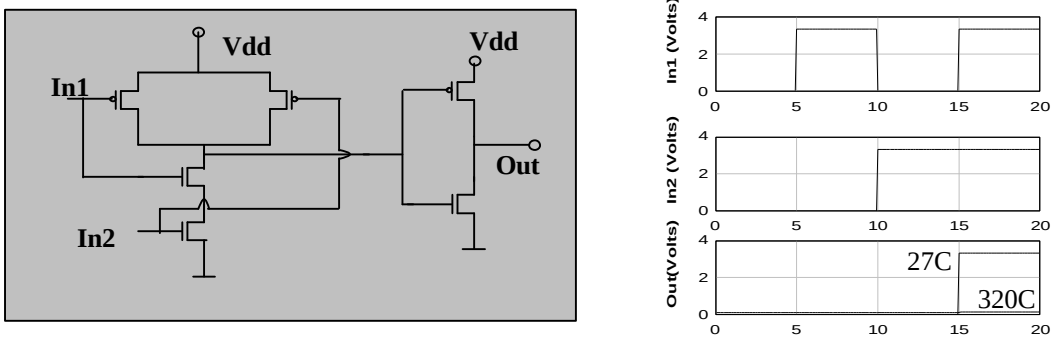


Figure 6 - Conventional AND gate and response at 27°C and 320°C. X axes of the graphs show time in ms.

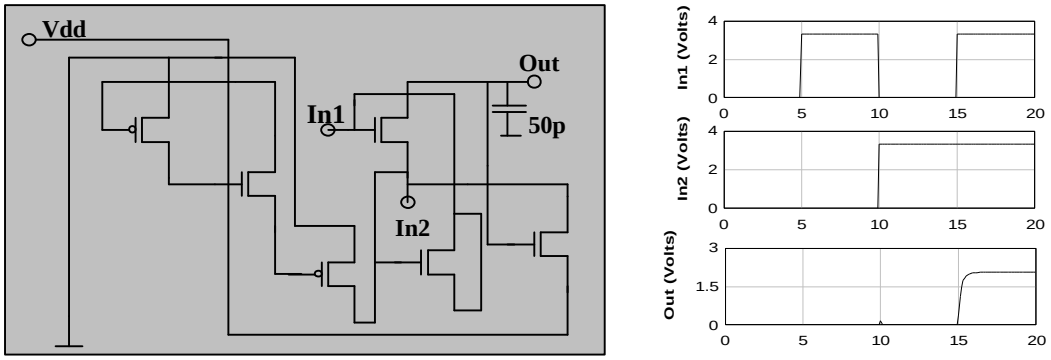


Figure 7 - Evolved AND gate at 320°C. X axes of the graphs show time in ms.